Abstract

A dual-channel memory system and accompanying coherency mechanism is disclosed. The memory includes both a request and a response channel. The memory provides data to a requester such as an instruction processor via the response channel. If this data is provided for update purposes, other read-only copies of the data must be invalidated. This invalidation may occur after the data is provided for update purposes, and is accomplished by issuing one or more invalidation requests via one of the memory request or the response channel. Memory coherency is maintained by preventing a requester from storing any data back to memory until all invalidation activities that may be directly or indirectly associated with that data have been completed.